

Claims 1-6 and 8-24 were rejected under 35 U.S.C. 102 as unpatentable over U.S. Patent No. 6,156,598 to Zhou et al. ("Zhou"). The rejection is respectfully traversed.

Claims 10-20 have been canceled with prejudice. Independent claim 1 has been amended to recite in part "anisotropically etching the mask layer to form a sidewall mask layer on sides of the gate electrode over the dielectric layer" and "isotropically etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer and a sidewall protection layer on sides of the gate electrode". Support for the amendment may be found in the specification, for example, at page 7, line 28 - page 8, line 7. Applicant respectfully submits that the Examiner has cited no portion of Zhou that describes or suggests a method including "anisotropically etching the mask layer" and isotropically etching the dielectric layer" as recited in claim 1, as amended. Accordingly, applicant respectfully submits that claim 1 is patentable over the cited art for at least the reasons stated above. Amendments have also been made to dependent claims 2-3 and 24. No new matter has been entered. Claims 2-6, 8-9 and 24 depend from claim 1 and are patentable for at least the same reasons as claim 1. Independent claim 21 can be distinguished in a similar manner as claim 1. Claim 22 depends from claim 21 and is patentable for at least the same reasons.

In view of the above, applicant respectfully submits that claims 1, 3-6, 8 and 21-24 are patentable over the cited art.

Claim 7 was rejected under 35 U.S.C. 103(a) as unpatentable over Zhou in view of U.S. Patent No. 6,180,472 to Akamatsu et al. ("Akamatsu"). The rejection is respectfully traversed. Claim 7 depends from claim 1. Applicant respectfully submits that the Examiner cited no portion of Akamatsu that overcomes the deficiencies of Zhou discussed above. Accordingly, for at least the above reason, claim 7 is patentable over the cited art.

New dependent claims 25-26 have been added. Support for the new claims may be found throughout the specification and drawings and in the original claims. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-9 and 21-26 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application

is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,



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Version With Markings to Show Changes Made

Claims 1-3 and 21-24 were amended as follows:

1. A method for manufacturing a semiconductor device, the method comprising:
 - (a) forming a gate dielectric layer over a semiconductor substrate;
 - (b) forming a gate electrode over the gate dielectric layer;
 - (c) forming a dielectric layer over the semiconductor substrate;
 - (d) forming a mask layer over the dielectric layer;
 - (e) anisotropically etching the mask layer to form a sidewall mask layer on sides of the gate electrode over the dielectric layer;
 - (f) isotropically etching the dielectric layer using the sidewall mask layer as a mask to form an extension control layer on sides of the gate dielectric layer; and
 - [(c) forming an extension control layer over the semiconductor substrate on sides of the gate dielectric layer; and]
 - [(d)] (g) forming a first impurity layer and a second impurity layer by ion-implanting an impurity in the semiconductor substrate,wherein an extension region is formed in the semiconductor substrate below the extension control layer during the ion-implanting used to form the first impurity layer and the second impurity layer.

2. (amended) A method for manufacturing a semiconductor device according to claim 1, wherein the step (f) [(c)] further includes the step of forming a sidewall protection [film] layer on sidewalls of the gate electrode [with the extension control layers].

3. (amended) A method for manufacturing a semiconductor device according to claim 2, [wherein the step (c)] further including [includes the steps of:

(c – 1) forming a dielectric layer over the semiconductor substrate;

(c – 2) forming a sidewall mask layer on sides of the gate electrode over the dielectric layer;

(c – 3) removing the dielectric layer using the sidewall mask layer as a mask to form the extension control layer and the sidewall protection layer; and

(c – 4)] removing the sidewall mask layer after the isotropically etching the dielectric layer and prior to the forming a first impurity layer and a second impurity layer [step (c – 3)].

21. (amended) A method for manufacturing a semiconductor device including extension regions and source/drain regions formed using a single ion-implantation step, the method comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a gate electrode over the gate dielectric layer;

forming extension control structures over a portion of the semiconductor substrate next to the gate dielectric layer by forming a dielectric layer on the semiconductor substrate, forming a mask layer on the dielectric layer, anisotropically etching the mask layer to form a sidewall mask layer, and isotropically etching the dielectric layer after forming the sidewall mask layer; and

[a single] an ion-implanting step that forms extension regions in the semiconductor substrate under the extension control structures and source/drain regions in the semiconductor substrate adjacent to the extension layer, wherein the extension regions have a depth that is less than that of the source/drain regions.

22. (amended) A method according to claim 21, further comprising forming sidewall protection structures on sidewalls of the gate electrode during the isotropically etching the dielectric layer [, wherein the sidewall protection structures are formed from the same material as the extension control structures].

23. (amended) A method according to claim 22, further comprising [wherein the extension control structures and sidewall protection structures are formed using a method comprising:

depositing a dielectric layer over the surface of the semiconductor substrate and the gate electrode;

forming a mask layer on the dielectric layer;

anisotropically etching the mask layer to form a sidewall mask layer;

etching the dielectric layer using the sidewall mask layer as a mask so that the dielectric layer remains at sidewalls of the gate electrode and extends a distance outward from the gate dielectric layer along the surface of the dielectric layer; and.]

removing the sidewall mask layer prior to the ion-implanting [;

wherein the dielectric layer remaining at sidewalls of the gate electrode defines the sidewall protection structures and the dielectric layer extending a distance outward from the gate dielectric layer along the surface of the dielectric layer defines the extension control structures].

24. (amended) A method of manufacturing a semiconductor device according to claim 1, wherein the extension control layer is formed from silicon nitride and the sidewall mask is formed from silicon oxide [a dielectric material].